

An apparatus and method for interfacing a processor to one or more co-processors interface is disclosed. The apparatus provides a dual ported memory to be used as a message passing buffer between the processor and the co-processor. Both the processor and co-processors can interface asynchronously to the dual ported memory. Control logic monitors activity by the processor to alert the co-processors of communications by the processor written to the memory and otherwise allow the processor and co-processors to think they are interfacing directly with one another.